Title: **JP05189383A2: MULTIPROCESSOR SYSTEM AND INTERFACE DEV**

Country: **JP** Japan
Kind: **A**

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Abstract:

PURPOSE: To connect an interface circuit to a system bus having a shared memory by providing the interface circuit with an input connected to a microprocessor device to receive an address signal line and a control signal line.

CONSTITUTION: A global memory state machine of a processor buffered interface 22c receives inputs from a DMA controller and an inter-processor communication register. The control signal line from a local state machine is connected to a local memory 22b, and the control signal line from the global memory state machine is connected to a global bus 24 through a local processor card bus 32 and a universal bus interface 24. The global memory state machine generates a global memory address and a control signal correspondingly to local processors 22a and 28a or in response to the operation of the DMA controller or the like.

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Other Abstract Info: DERABS G93-046873